Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A high-speed signal processor which functions as a waveform acquisition system and a high-speed analog-to-digital converter, said processor comprising:

a filter system for dividing ~~an~~ a single input signal into a series of adjacent frequency bands;

a frequency down converter for down converting one or more of the adjacent frequency bands as they are output from said filter system;

a digitizer for digitizing each frequency band output from said filter system; and

a system for reconstructing the original input signal.

2. (Canceled)

3. (Original) The high-speed signal processor as recited in Claim 1, wherein said filter system comprises an M-band filter bank.

4. (Original) The high-speed signal processor as recited in Claim 3, wherein the M-band filters in said M-band filter bank enable perfect reconstruction, meaning that the sum of the cascaded responses of the M-band analysis filters followed by the synthesis filters produces an overall flat amplitude response and group delay.

5. (Original) The high-speed signal processor as recited in Claim 3, wherein the M-band filters in said M-band filter bank are implemented optically using fiber optics.

6. (Original) The high-speed signal processor as recited in Claim 3, wherein the M-band filters in said M-band filter bank are implemented electronically.

7. (Original) The high-speed signal processor as recited in Claim 3, wherein the M-band filters in said M-band filter bank are implemented using software.

8. (Original) The high-speed signal processor as recited in Claim 3, wherein each channel output is equalized, to thereby shape the transfer function of the channel into that of an M-band filter.

9. (Original) The high-speed signal processor as recited in Claim 8, wherein the channel equalization is implemented with Weiner filter technology.

10. (Original) The high-speed signal processor as recited in Claim 1, wherein a calibration signal is continuously injected into said processor to serve as a reference for quantifying and removing hardware errors.

11. (Currently Amended) A method for processing signals, comprising :

dividing ~~an~~ a single input signal into a series of adjacent frequency bands;

down-converting each frequency band to allow each band to be sampled at a lower rate;

digitizing each frequency band; and

reconstructing the original input signal.

12. (New) The method as recited in Claim 11, wherein said dividing step is performed using filters having a perfect reconstruction property.

13. (New) The method as recited in Claim 11, and further comprising a step of injecting a calibration signal such that it passes through a common point with the single input signal, prior to the performance of the dividing step.

14. (New) The method as recited in Claim 11, wherein none of the steps involve removing noise supplied in the single input signal.

15. (New) The high-speed signal processor as recited in Claim 10, wherein said calibration signal is injected in a manner such that it passes through the same point as said single input signal, in front of said filter system.

16. (New) The high-speed signal processor as recited in Claim 1, wherein the system does not function to remove noise supplied in the single input signal.

17. (New) A high-speed signal processor which functions as a waveform acquisition system and a high-speed analog-to-digital converter, said processor comprising:

a filter system for dividing an input signal into a series of adjacent frequency bands, comprising an M-band filter bank;

a digitizer for digitizing each frequency band output from said filter system; and

a system for reconstructing the original input signal;

wherein the M-band filters in said M-band filter bank enable perfect reconstruction, meaning that the sum of the cascaded responses of the M-band analysis filters followed by the synthesis filters produces an overall flat amplitude response and group delay.